CLAIMS

What is claimed is:

1. A method comprising:

receiving a write request;

receiving a read request; and

preempting write data with the read request.

2. The method according to claim 1, wherein the read request is within a write packet.

3. The method according to claim 1, wherein the read request preempting the write data is received in time after the write request.

4. The method according to claim 1, wherein the read request and write request each have an associated link layer control.

5. The method according to claim 1, wherein the read request is selected from the group consisting of a memory read request, a device read request, and a configuration read request.

6. The method according to claim 1, wherein the write request is selected from the group consisting of a memory write request, a device write request, and a configuration write request.

7. An apparatus comprising:

a memory system having an input, an output, and a control;

a memory port having a memory input, a memory output, a memory control, a processor input, a processor output, and a processor control, wherein the memory system input is coupled to receive the memory port memory output, the memory port memory input is coupled to receive the memory system output, and the memory system control is coupled to the memory port memory control, and

a processor having an memory output, a memory input, and a memory control, wherein the memory port processor input is coupled to receive the processor memory output, the processor memory input is coupled to receive the memory port processor output, and the processor memory control is coupled to the memory port processor control.

8. The apparatus of claim 7, wherein the memory port has a memory port protocol allowing a processor write request to be preempted by a processor read request.

9. The apparatus of claim 8, wherein the memory port protocol further comprises a payload packet and an associated link layer control packet.

10. A machine-readable medium having stored thereon instructions, which when executed causes a system to:

issue a write request;

issue a read request; and

preempt write data with the read request.

11. The machine-readable medium according to claim 10, wherein the read request is within a write packet.

12. The machine-readable medium according to claim 10, wherein the read request and the write request each further comprise an associated link layer control.

13. A system comprising:

a processor capable of issuing a read request, and a write request; and

a memory device coupled to the processor wherein processor write data is preempted by the processor read request.

14. The system of claim 13, wherein the processor read request can be issued within a write packet.

15. The system of claim 13, wherein the read request and write request each further comprise an associated link layer control.

16. An apparatus comprising:

means for receiving a write request;

means for receiving a read request; and

means for preempting write data with the read request.

17. The apparatus of claim 16, wherein means for preempting the write data with the read request is a means for receiving a link layer control associated with the read request.

18. The apparatus of claim 16, wherein means for preempting the write data with the read request is a means for receiving a link layer control associated with the write request.

19. A method comprising:

receiving a read request flit; and

dispatching an early read request to a memory.

20. The method according to claim 19, wherein dispatching the early read request to the memory occurs after receiving a first half of the read request flit.

21. The method according to claim 20, wherein the first half of the flit has an indicator for early dispatch of the early read request to the memory.

22. The method according to claim 21, wherein the indicator for early dispatch of the read request is selected from the group consisting of early dispatch of read allowed and early dispatch of read not allowed.

23. An apparatus comprising:

a memory system having an input, an output, and a control; and

a memory port having a memory input, a memory output, and a memory control, wherein the memory system input is coupled to receive the memory port memory output,

the memory port memory input is coupled to receive the memory system output, and the memory system control is coupled to the memory port memory control.

24. The apparatus of claim 23, wherein the memory port has a memory port protocol supporting an early read request.

25. The apparatus of claim 24, wherein the early read request is located within a first half of a read request flit.

26. A machine-readable medium having stored thereon instructions, which when executed causes a system to:

receive a read request flit; and

dispatch a read request to a memory.

27. The machine-readable medium according to claim 26, wherein dispatching the read request to the memory occurs before receiving the entire read request flit.

28. The machine-readable medium according to claim 27, wherein the first half of the flit has an indicator for early dispatch of the read request to the memory selected from the group consisting of early dispatch of read allowed and early dispatch of read not allowed.

29. A system comprising:

a processor capable of issuing an early read request; and

a memory device coupled to the processor capable of receiving the early read

request and performing an early read of a memory.

30. The system of claim 29, wherein the processor early read request is issued within a first half of a read request flit packet.

31. The system of claim 30, wherein the first half of the read request flit packet has an indicator for early dispatch of the read request to the memory device selected from the group consisting of early dispatch of read allowed and early dispatch of read not allowed.

32. An apparatus comprising:

means for issuing an early read request; and

means for a memory device to receive the early read request and perform an early read of a memory.

33. The apparatus of claim 32, wherein means for issuing an early read request is a means for setting an indicator in a first half of a read request flit.

34. The apparatus of claim 32, wherein means for performing the early read of the memory is controlled by an indicator selected from the group consisting of early dispatch of read allowed and early dispatch of read not allowed.

35. A method comprising:

receiving a first half of a read request flit; and

dispatching a read request to a memory.

36. The method according to claim 35, wherein dispatching the read request to the memory occurs before receiving a second half of the read request flit.

37. The method according to claim 35, wherein dispatching the read request to the memory occurs before error checking an entire read request flit.